Total No. of Questions : 12]

SEAT No. :

P857

[Total No. of Pages : 3

[4659]-236

B.E. (Computer) (Semester -II)

ADVANCED COMPUTER ARCHITECTURE

(2008 Pattern)

Time : 3Hours] *[Max. Marks :100*

Instructions to the candidates:

1) ***Answer three questions from Section I and three questions from Section II.***
2) ***Answers to the two sections should be written in separate books.***
3) ***Neat diagrams must be drawn wherever necessary.***
4) ***Figures to the right indicate full marks.***
5) ***Assume suitable data, if necessary.***

SECTION-I

Q1) a) Explain in brief general classification of parallel computer architectures based on following techniques. **[8]**

i) Flynn's classification

ii) Feng's classification

b) With suitable example/flow chart explain: **[8]**

i) Branch Prediction and

ii) Speculative loading

OR

Q2) a) Define parallel processing. How parallel computer architectures are classified? Discuss the levels of parallel processing. **[8]**

b) What is EPIC? Explain EPIC features of Itanium processor in details. **[8]**

Q3) a) With the help of the block diagram explain in detail branch prediction logic implemented in Pentium architecture. **[8]**

b) Explain various types of data hazards observed in Pentium processor. How these hazards could be detected? **[8]**

OR

P.T.O.

Q4) a) Explain in brief register window structure of SPARC. How it supports parameter passing through procedure calls? **[8]**

b) Discuss the various features of UltraSPARC architecture. Explain in brief, the concept of RSE. **[8]**

Q5) a) Discuss with suitable example the necessity of Data routing and manipulation with respect to SIMD interconnection network. Also define data routing functions of 3 cube network. **[10]**

b) For a Mesh interconnection network for array processors, discuss in detail the parallel algorithm for matrix multiplication. Obtain the time complexity for the same. **[8]**

OR

Q6) a) How a 3-cube network can be viewed as **[6]**

i) Single stage recirculating network.

ii) Multistage network.

b) Discuss parallel sorting algorithm for array processors and obtain its time complexity. **[6]**

c) With suitable example explain following features implemented in cray-1 architecture. **[6]**

i) Vector chaining.

ii) Vector looping.

SECTION-II

Q7) a) What is the difference between static and dynamic bus arbitration techniques. Explain any two dynamic bus arbitration techniques. **[8]**

b) Explain in brief desirable processor characteristics for multiprocessor architecture. **[8]**

OR

Q8) a) Explain features of IBM Power 4 Processor. **[8]**

b) Explain time shared bus as an interconnection network for multiprocessor systems. Discuss daisy chaining arbitration algorithm, with neat diagram. **[8]**

Q9) a) Discuss the various context switching policies implemented in multithreaded architecture. **[8]**

b) Explain with suitable example shared memory parallel programming. **[8]**

OR

Q10)a) Discuss different latency hiding techniques used in multithreading architectures. **[8]**

b) Explain in brief the following with respect to multithreading: **[8]**

i) Latency.

ii) Context switched overhead.

iii) Interleaved multithreading.

iv) Number of threads.

Q11)a) Discuss the issues in multiprocessor operating system? Discuss in detail. **[10]**

b) What is the difference between grid computing and cluster computing? Discuss features of grid computing. **[8]**

OR

Q12)a) What are various performance measures for the parallel algorithms? **[6]**

b) Comment on PThreads (parallel threads) in shared memory system? **[6]**

c) What are the major features of FOR TRAN-90 to be qualified as parallel programming language? **[6]**

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